In the claims

1. (Previously presented) Apparatus for interfacing a media access controller (MAC) and a physical layer device (PHY) for operating as either a gigabit media independent interface or a ten bit interface, transferring data at a predetermined clock rate while substantially reducing the required number of input and output pins, said apparatus comprising:

a multiplexer for mapping data and control signals that are normally applied to a predetermined number of pins to a lesser number of pins.

2. (Previously presented) Apparatus as defined in claim 1 wherein said multiplexer multiplexes different significant bits of data on the same set of pins using both edges of a clock signal having the predetermined rate, thereby transferring data at the predetermined rate on the lesser number of pins.

3. (Original) Apparatus as defined in claim 2 wherein the clock rate is within the range of about 2.5 MHz and about 125 MHz, with the clock rate being within the range of about 2.5 and about 25 MHz for the ten bit interface and about 125 MHz for the gigabit media independent interface operation.

4. (Previously presented) Apparatus as defined in claim 2 wherein said multiplexer controls the relative timing between the clock signal and the data during transmitting and during receiving, the clock and data signals being generated substantially simultaneously when either the MAC or the PHY transmits the signals, such that the data to clock output skew at the transmitter is within +/- 500 picoseconds and the data to clock input skew at the receiver is between about 1 and about 2.8 nanoseconds for clock signal speeds within the range of 2.5 MHz and 125 MHz.

5. (Original) Apparatus as defined in claim 3 wherein the clock signal has a duty cycle for gigabit media independent interface operation that is within the range of 45 and 55 percent and a duty cycle for the ten bit interface operation that is within the range of 40 and 60 percent.

6. (Previously presented) Apparatus for interfacing a media access controller (MAC) and a physical layer device (PHY) for operating as at least one of a gigabit media independent interface and a ten bit interface, transferring data at a predetermined clock rate while substantially reducing the required number of input and output pins, said apparatus comprising:

a multiplexer for mapping data and control signals that are normally applied to a predetermined number of pins to a lesser number of pins; and

six input pins for use in either the gigabit media independent interface operation or the ten bit interface operation in which:

a transmit reference clock signal TXC is applied to a first pin in the gigabit media independent interface operation and the ten bit interface operation;

8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation;

2 bits of data are applied to the sixth pin in the ten bit interface operation; and,

control signals are applied to the second through fifth pin in the gigabit media independent interface operation.

7. (Previously presented) Apparatus for interfacing a media access controller (MAC) and a physical layer device (PHY) for operating as at least one of a gigabit media independent interface and a ten bit interface, transferring data at a predetermined clock rate while substantially reducing the required number of input and output pins, said apparatus comprising:

a multiplexer for mapping data and control signals that are normally applied to a predetermined number of pins to a lesser number of pins; and

six output pins for use in either the gigabit media independent interface operation or the ten bit interface operation in which:

a receive reference clock signal RXC is derived from the received data stream and appears on a first pin in the gigabit media independent interface operation and the ten bit interface operation;

8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation;

2 bits of data are applied to the sixth pin in the ten bit interface operation; and,

control signals are applied to the second through fifth pin in the gigabit media independent interface operation.

8. (Previously presented) A media interface for a media access controller (MAC) and a physical layer device (PHY) for operating as at least a gigabit media independent interface and a ten bit interface, which interface transfers data responsive to receiving a clock signal having a predetermined clock rate on a reduced number of pins, said interface multiplexing the data and control signals that are applied to the reduced number of pins using both edges of said clock signal and for selectively mapping the data and control signals to the reduced number of pins, wherein CRS and COL control signals are applied on a single pin.

9. (Previously presented) A media interface as defined in claim 8 wherein the reduced number of pins is 13.

10. (Previously presented) A media interface for a media access controller (MAC) and a physical layer device (PHY) for operating as at least a gigabit media independent interface and a ten bit interface, which interface transfers data responsive to receiving a clock signal having a predetermined clock rate on a reduced number of pins, said interface multiplexing the data and control signals that are applied to the reduced number of pins using both edges of said clock signal and for selectively mapping the data and control signals to the reduced number of pins;

six input pins for use in either the gigabit media independent interface operation or the ten bit interface operation in which:

a transmit reference clock signal TXC is applied to a first pin in the gigabit media independent interface operation and the ten bit interface operation;

8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation;

2 bits of data are applied to the sixth pin in the ten bit interface operation; and,

control signals are applied to the second through fifth pin in the gigabit media independent interface operation.

11. (Previously presented) A media interface for a media access controller (MAC) and a physical layer device (PHY) for operating as at least a gigabit media independent interface and a ten bit interface, which interface transfers data responsive to receiving a clock signal having a predetermined clock rate on a reduced number of pins, said interface multiplexing the data and control signals that are applied to the reduced number of pins using both edges of said clock signal and for selectively mapping the data and control signals to the reduced number of pins;

six output pins for use in either the gigabit media independent interface operation or the ten bit interface operation in which:

a receive reference clock signal RXC is derived from the received data stream and appears on a first pin in the gigabit media independent interface operation and the ten bit interface operation;

8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation;

2 bits of data are applied to the sixth pin in the ten bit interface operation; and,

control signals are applied to the second through fifth pin in the gigabit media independent interface operation.

12. (Previously presented) Apparatus as defined in claim 1 wherein CRS and COL control signals are applied on a single pin.

13. (Previously presented) A method of interfacing a media access controller (MAC) and a physical layer device (PHY) for operating either as a gigabit media independent interface or a ten bit interface, and transfer data at a predetermined rate while substantially reducing the required number of input and output pins, said method comprising:

multiplexing data and control signals using both edges of a clock signal having the predetermined rate; and,

strategically mapping the data and control signals that are normally applied to a predetermined number of pins to a significantly lesser number of pins while still maintaining the operability of the interface.